Notice of Allowability	Application No.	Applicant(s)	
	09/625,996	ADAMS ET AL.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/12/2004*.

2. ☒ The allowed claim(s) is/are *1,3-8 and 10-17*.

3. ☒ The drawings filed on *30 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Guy J. LAMARRE
PRIMARY EXAMINER

REASONS FOR ALLOWANCE

Claims 1, 3-8 and 10-17 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches a integrated circuit including an embedded memory and a built-in self-test arrangement comprising means for storing test instructions and discriminating between performing manufacturing level or board level testing and system level testing based on receiving test instructions provided from an external tester, means for generating default test instructions for performing system level testing when test instructions are not provided by said external tester, and means for supplying said default test instructions for performing system level testing to said means for storing test instructions, wherein said means for generating default test instructions includes an initialization storage means for providing signals for initializing said means for storing test instructions in the absence of said test instructions provided from an external tester. The foregoing limitations are not explicitly found in the prior arts of record, nor are they obvious.

The prior art of record, namely Schwarz, teaches a reconfigurable built-in self-test circuit for enabling the debugging of an embedded device. In one embodiment, the write data path from the built-in self-test module to the embedded device includes a multiplexer, which is controlled by a debug signal. When the debug signal is de-asserted, the multiplexer forwards the write data from the built-in self-test module to the embedded device, thereby allowing the self-test to proceed in the hard wired manner. When the debug signal is asserted, the multiplexer forwards external data from the user to the embedded device, thereby allowing the user to execute customized tests on the embedded device. A second multiplexer is similarly placed in the

expected data path from the built-in self-test module to the comparator to allow the user to provide external data for comparison with output data from the embedded device when the debug signal is asserted. For all tests, the address and control data is provided by the built-in self-test module to avoid the need to implement an external access to these data paths. Schwarz teaches (Figure 2) a functional block diagram of integrated circuit 200 with an improved BIST configuration. The improved BIST configuration includes multiplexers 202, 204 and a buffer 206. Multiplexers 202,204 are controlled by an external debug signal. When the debug signal is de-asserted, multiplexer 202 routes data patterns from BIST 104 to RAM 102, and multiplexer 204 routes expected data from BIST 104 to comparator 106. And when the debug signal is asserted, multiplexer 202 routes data patterns from external data buffer 206 to RAM 102, and multiplexer 204 routes expected data from external data buffer 206 to comparator 106. In normal operation the debug signal is de-asserted, and there is no change in how the BIST operates from a conventional BIST. However, when a part requires debugging it is possible to modify the pattern data and expected data seen by RAM 102. This is accomplished by asserting the debug signal, which brings the data buses under external control. During a write cycle multiplexer 202 will select the external data bus as the data pattern provided to the RAM 102. Similarly, during a read cycle, multiplexer 204 will select the external data bus as the expected data for comparator 106. The external data bus instrument by buffer 206 which is driven by the user provided external data signal. In this manner the data written to RAM 102 can be controlled by the user. None of the prior arts of record teach nor fairly suggest all the limitations in the independent claim 1 of the present application. In particular, the limitations of "...means for storing test instructions and discriminating between performing manufacturing level or board level testing

and system level testing based on receiving test instructions provided from an external tester, means for generating default test instructions for performing system level testing when test instructions are not provided by said external tester, and means for supplying said default test instructions for performing system level testing to said means for storing test instructions, wherein said means for generating default test instructions includes an initialization storage means for providing signals for initializing said means for storing test instructions in the absence of said test instructions provided from an external tester" are not taught nor fairly suggested in the prior arts of record.

Independent claims 8 and 17 include similar limitations of independent claim 1 and therefore are allowed for similar reasons.

Dependent claims 3-7 and 10-16 depend from independent claims 1 and 8 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
November 6, 2004

GUY J. LAMARRE
PRIMARY EXAMINER